

CURRICULUM – VITAE

Ms.Binal J.Jadawala

Date of Birth: December 31, 1987

Indian, Female

Permanent Address:

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Present Status

- Presently working as a Lecturer in E. & C. Engineering Department, B. & B. Institute of Technology, Vallabh Vidyanagar since 9th June 2011.

Work Experience

- Total teaching experience is 5 years.

Academics

M. E. (Communication Engineering)

G. H. Patel College of Engineering & Technology, Vallabh Vidyanagar (G.T.U).
PURSUING

B.E. (Electronics Engineering)

Birla Vishvakarma Mahavidhyalaya,V.V.Ngar,(S.P.U)
C.P.I(6.79)

H.S.C. (10 + 2) (Science Stream)

Gujarat Higher Secondary Education Board
Percentage: 63.69%
March 2005.

S.S.C. (10th)

Gujarat Secondary Education Board
Percentage: 87.86%
March 2003.

Skill Set:

Languages

C.

Simulation Tool	MATLAB, Quartus-II, Multisim, Orcad.
Protocol	TCP/IP.
OS	Windows, DOS.
Assembly Language	8085 and 8086 Microprocessor, 80C51 Micro controller.

Workshop / Training Programme / Seminar / STTP Attended

Total No.: 2 STTP Attended.
2 Workshop attended.

Subject Taught At Diploma Level

- Electronics Devices & Circuits – I.
- Electronics Devices & Circuits – II.
- Electronics Component And Practice.
- Television Engineering.
- Fiber Optic Communication.
- Electronics Networks And Lines
- Computer Networks.

Co-Curricular Activities

- Worked for Admission Registration.
- Worked for Annual Function in Institute.

Reference

Mr. M. Y. Kantharia
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